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Modelling and Simulation of Bridgeless SEPIC PFC Rectifier Operating in Continuous Conduction Mode

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Abstract

Nowadays, bridgeless circuits are gaining more popularity due to less harmonic distortion of current in the input due to absence of input diode bridge circuit. A SEPIC PFC converter is capable of operating in both step-up and step-down mode. In this paper modelling of a bridgeless SEPIC PFC converter operating in Continuous Conduction Mode with single switch using State SSA technique is presented. In the proposed converter due to presence of complex poles and zeros which makes the system unstable and leads to difficult design of stable control.
The paper also shows the modified circuit and their modelling using suitable damping network for the achievement of stability. Simulation results are presented to verify the accuracy of the model.

Keywords:

Bridgeless;
Continuous conduction mode;
Modelling;
Power factor corrector;
Rectifier;
SEPIC;
Single switch;

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1. Introduction

The most popular PFC topology is the boost converter which is simple for power and control point of view. But due to their limitation i.e., its output voltage must be greater than its peak input voltage it cannot be used for the application where output voltage less than its input voltage required. So a Single Ended Primary Inductor Converter (SEPIC) can be preferable due to its Step-Up and Step-Down property to overcome the limitation of boost topologies.

Bridgeless PFC topologies are gaining more popularity due to better thermal management, less conduction losses and low harmonic distortions and improved efficiency compared to conventional PFCs [3,2]. Several bridgeless PFC topologies for boost PFCs and SEPIC PFCs were introduced [1, 2, 10] in which two MOSFETs were used with high ultra fast diodes. Among different topologies the topology shown in Fig.1a. and Fig.1.b has better performance in terms of Power Factor, THD and efficiency [2].

These topologies uses two switches with bridgeless SEPIC topology So the two switch configuration can be modified with a single switch as shown in Fig.2 to achieve the better result interns of less switching losses,

conduction losses and better thermal management and improved efficiency as compared to existing topologies due to fewer components in the current conduction path.

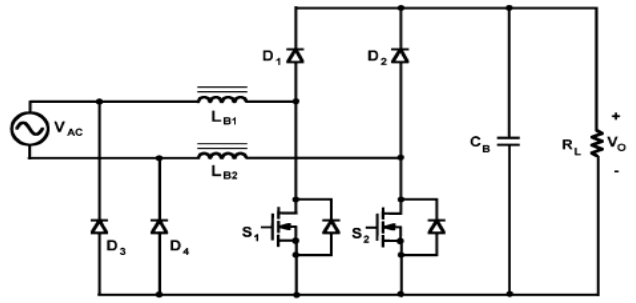

Fig.1.a. Bridgeless PFC rectifier Boost topology [2]

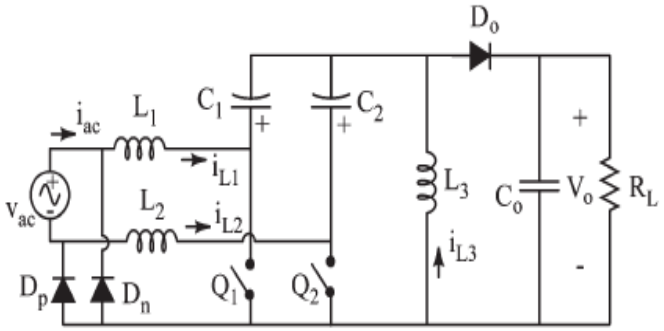

Fig.1.b. Bridgeless PFC rectifier SEPIC topology [1]

The conventional SEPIC converter has an active power switch, two inductors, a diode and two capacitors and is thus a fourth order non linear system [4]. Due to presence of un-damped complex poles and zeros the system leads to unstable condition resulting difficult to design a stable feedback controller.

To overcome this problem it need to be modified with a proper damping network which will properly shape the current loop transfer function [5]. This paper focuses on the modelling and simulation of the proposed converter Fig.2 operating in continuous conduction mode with and without the damping network.

2.Proposed Bridgeless SEPIC PFC Converter

Fig.2. shows a bridgeless SEPIC PFC converter which has a single active switch. The topology constructed using two dc-dc converters. During positive half line period the 1st dc-dc converter L_1-C_1-Lo-Do is active through D_p . During the negative half line cycle 2nd dc-dc converter L_2-C_2-Lo-Do is active through diode D_n .

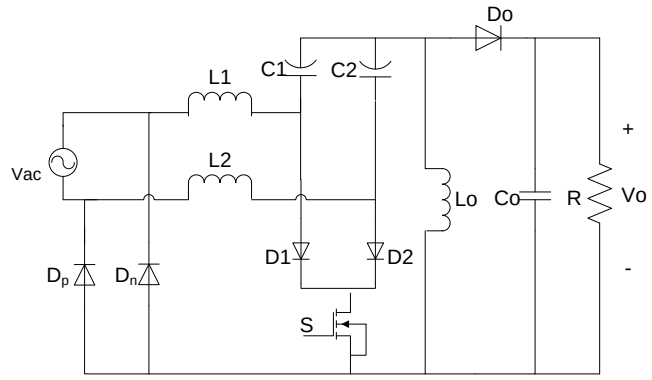

Fig.2.Proposed bridgeless single switch SEPIC PFC converter

As each dc-dc converters operates either in positive or negative half line cycle the converter has symmetry in nature. Thus In this paper only positive half line period is taken for the analysis.

From Fig.2.it can be observed that two additional diodes D1and D2 are used at the cost of single switch. But it can be shown in the next section that only one diode is in the current conduction path. Hence it does not increase the conduction losses.

3. Opeartional Mode Analysis

As the converter operates in Continuous Conduction Mode it has only two stable states i.e., switch-ON and switch-OFF states.

A. Switch-ON State:

Fig.3.a. shows switch on time circuit topology for which Switch S is ON and output diode Do is OFF.

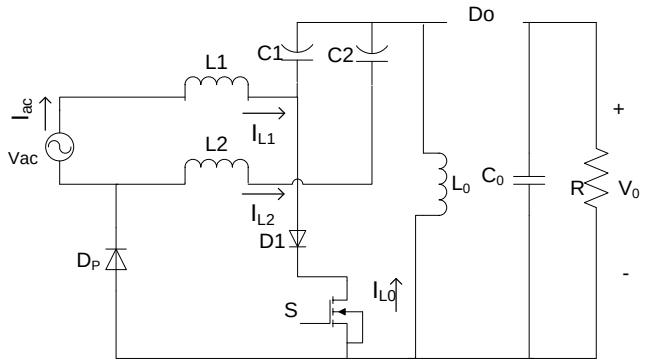

Fig. 3.a. Switch-ON topology

In this stage L_1 is charged from input voltage and C_1 transfer its energy to output inductor Lo and Lo is charging at this stage. As S_1 is ON and C_1 is only charging diode D_1 is only conducting with input line diode D_P. Although the desired sensing current is the only current through L1,the actual sensing current is the sum of currents flowing into L1 and L2. In the positive half line period L2 is left uncontrolled.

B. *Switch-OFFState:*

Fig. 3.b. shows switch OFF time circuit topology for which S is OFF and output diode Do is ON. At this stage C_1 is charged from L_1 to provide the output current. As switch S is in OFF state both diodes D_1 and D_2 are non-conducting at this stage. So as in both switching periods only two diodes are conducting resulting less conduction losses.

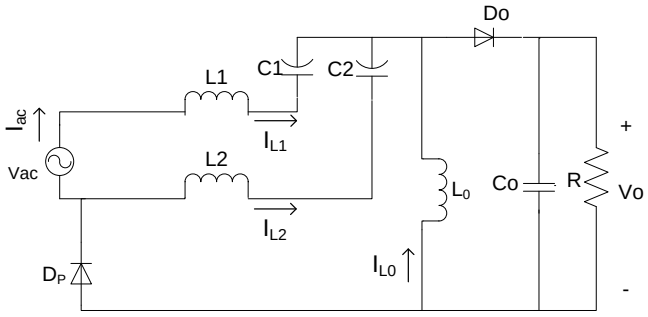

Fig. 3.b. Switch-OFF topology

4. Modelling of Proposed Converter

From Fig.3.a during switch ON of the switch S writing the voltage and current equations

$$L_1 \frac{di_{L1}}{dt} = V_{in} \qquad (1)$$

And $L_0 \frac{di_{L0}}{dt} = V_{C1} = V_{in}$ (2)

Now the current across C_1 is $i_{C1} = -i_{L0}$

i.e., $C_1 \frac{dV_{C1}}{dt} = -i_{L0}$ (3)

And current across C_0 is $i_{C0} = -i_0$

i.e., $C_0 \frac{dV_{C0}}{dt} = -\frac{V_0}{R} = -\frac{V_{C0}}{R}$ (4)

From Fig.3.b. during switch OFF interval of the switch S writing the voltage and current equations

$$L_1 \frac{di_{L1}}{dt} = V_{in} - V_{C1} - V_{C0} \qquad (5)$$

And $L_0 \frac{di_{L0}}{dt} = -V_{C0}$ (6)

Now the current through C_1 is $i_{C1} = i_{L1}$

i.e., $C_1 \frac{dV_{C1}}{dt} = i_{L1}$ (7)

And $i_{C0} = i_{L1} + i_{L0} - i_{C0}$

$$\Rightarrow C_0 \frac{dV_{C0}}{dt} = i_{L1} + i_{L0} - \frac{V_{C0}}{R} \quad (8)$$

Now defining states of the converter as following: $x_1 = i_{L1}, x_2 = i_{L0}, x_3 = V_{C1}, x_4 = V_{C0}$ And $U = V_{in}$, $Y = V_0$,

Using state space analysis the state space equation for switch ON period (using equation 1 to 4) can be written as

$$\dot{x} = A_1 x + B_1 U \quad (9)$$

Where $x = \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \end{bmatrix} = \begin{bmatrix} i_{L1} \\ i_{Lo} \\ V_{C1} \\ V_{C0} \end{bmatrix}$, (10)

$$A_1 = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{C_1} & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{RC_0} \end{bmatrix}, B_1 = \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_0} \\ 0 \\ 0 \end{bmatrix} \quad (11)$$

Similarly using equations (5) to (8) the state space equation during switch OFF period can be written as

$$\dot{x} = A_2 x + B_2 U$$

Where $A_2 = \begin{bmatrix} 0 & 0 & -\frac{1}{L_1} & -\frac{1}{L_1} \\ 0 & 0 & 0 & -\frac{1}{L_0} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ \frac{1}{C_0} & \frac{1}{C_0} & 0 & -\frac{1}{RC_0} \end{bmatrix}, B_2 = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix}$ (12)

5. State Space Averaging Model

There are several methods are available for model averaging such as: PWM switching modelling, circuit averaging method and State Space Averaging (S.S.A) model method [4, 6, 7]. In this paper the proposed converter's averaging model is obtained by using State Space Averaging technique.

As the converter operates in continuous conduction mode(CCM) it has only two stable states during one switching period T in which switch S has ON time i.e., D×T and OFF time i.e. (1-D)×T ,where D is the duty cycle.

Now the state space equation over complete one cycle can be written as

$$\dot{x} = Ax + BU = (A_1 D + A_2 D')x + (B_1 D + B_2 D')U \quad (13)$$

and Y=CU

Using small signal analysis the following transfer function can be obtained [4, 9]

$$\frac{x(s)}{d(S)} = (sI - A)^{-1}\{(A_1 - A_2)x + (B_1 - B_2)U\} \quad (14)$$

Using equation (14) different transfer function can be obtained

In this paper control to inductor current transfer function is used for analysis and validation purpose.

For evaluating the performance of the proposed converter with power stage specification of 150W/60V at 120 V_{rms} line voltage at 100 KHz switching frequencyis designed with following parameters [8].

L_1=490µH, L_2=490µH, Lo=490µH,C_1=C_2=0.5µF and C_3=2mF.

A. Frequency Response Analysis

With above power stage specification parameters and state vectors for both switching period (Equ.11-12) the following control to inductor transfer function (G_{di}) is obtained using MATLAB

$$G_{di}(s) = \frac{283000s^3 + 5.07*10^9 s^2 + 98.1s + 3.92*10^{15}}{s^4 + 20s^3 + 8.31*10^8 s^2 + 1.66*10^{10} s + 3.26*10^{14}} \quad (15)$$

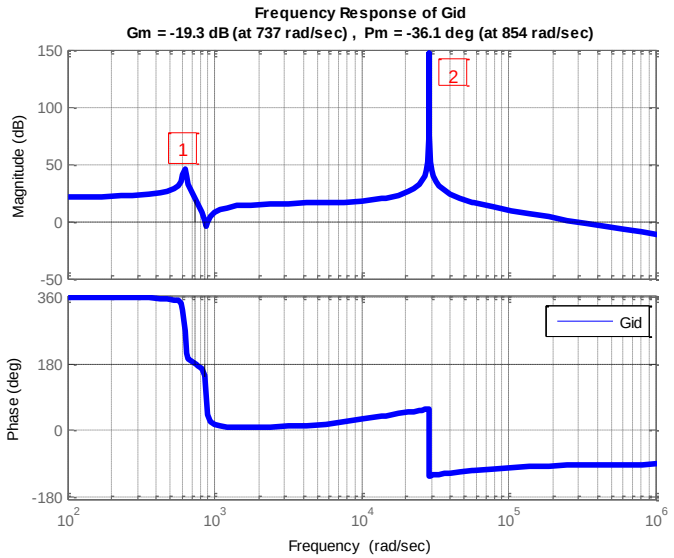

Fig.4 Frequency response of the derived transfer function G_{id}(Equ.15)

From figure 4 it can be observed that has two resonance points. The second resonance point has high Q-factor. This system has un-damped complex poles and zeros. Due to these reasons it results more oscillation in the input current and so as the unstable system which can be verified with the transfer function response's gain margin and phase margin.

To overcome this issue the proposed converter is modified with proper damping circuit [5]

6. Modelling of the Modified Converetr

In order to shape the transfer function a damping network i.e., R_d series with C_d connected paralleled with both C_1 and C_2. The basic operation of all the parameter remains same except R_d and C_d connected parallel

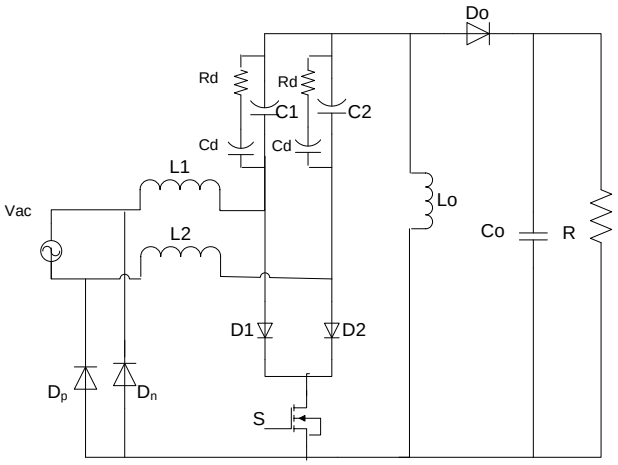

Fig.5 Modified proposed converter with damping network

across C_1 resulting the current divides into L_0 and Rd-C_d as well. Due to introduce of C_d the system is now getting 5th order

A. Operational Mode Analysis of Modified converter

*1) Switch-ON State:*Fig..5.a shows switch on time

circuit topology for which Switch S is ON and output diode Do is OFF. The basic operation of all the parameter remains same as that of proposed converter Fig.2 except R_d and C_d connected parallel across C_1 resulting in the current divides into L_0 and R_d-C_d as well.

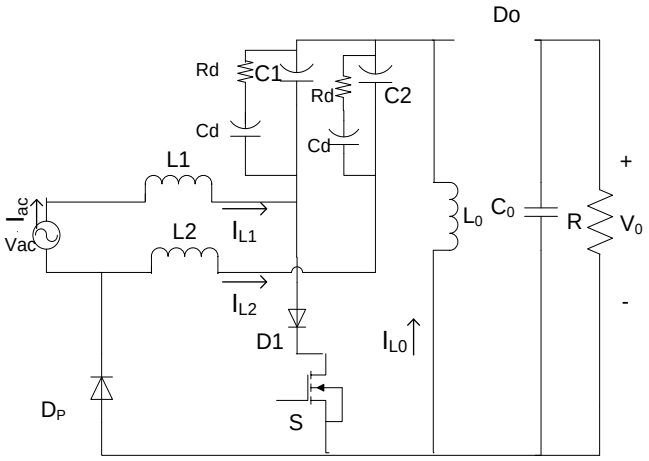

Fig..5.a Switch ON time circuit topology of modified converter

During switch ON period of the switch S writing the voltage and current equations

$$L_1\frac{di_{L_1}}{dt}=V_{in} \quad (16)$$

and $$L_0\frac{di_{L_0}}{dt}=V_{C_1}=V_{in} \quad (17)$$

Using KCL $$C_1\frac{dV_{C_1}}{dt}+i_{L_0}+\frac{V_{C_1}-V_{C_d}}{R_d}=0$$

$$\Rightarrow C_1\frac{dV_{C_1}}{dt}=-i_{L_0}-\frac{V_{C_1}-V_{C_d}}{R_d} \quad (18)$$

but $$C_d\frac{dV_{C_d}}{dt}=\frac{V_{C_1}-V_{C_d}}{R_d} \quad (19)$$

At the output node

$$C_0\frac{dV_{C_0}}{dt}=-\frac{V_{C_0}}{R}=-\frac{V_0}{R} \quad (20)$$

2) Switch-OFF State:

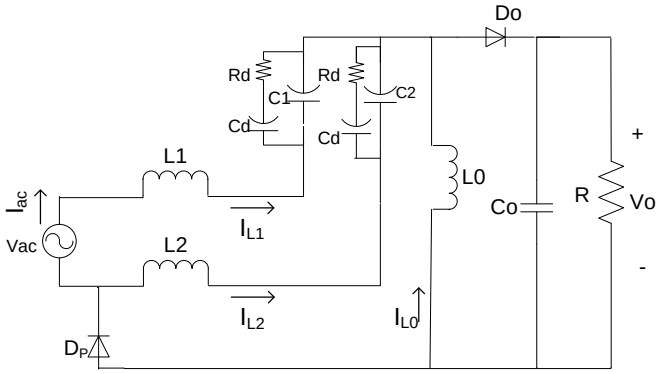

Fig.5.b. Switch OFF time circuit topology of modified converter

During switch-OFF period of the switch S writing the voltage and current equation

$$L_1\frac{di_{L_1}}{dt}=V_{in}-V_{C_1}-V_{C_0} \quad (21)$$

and $$L_0\frac{di_{L_0}}{dt}=-V_{C_0} \quad (22)$$

Applying KCL at the nodes

$$C_1\frac{dv_{c1}}{dt} = i_{L1} - \frac{V_{C1} - V_{Cd}}{R_d} \quad (23)$$

and $$C_0\frac{dv_{c0}}{dt} = i_{L1} + i_{L0} - \frac{V_{C0}}{R} \quad (24)$$

now the current through C_d is

$$C_d\frac{dV_{Cd}}{dt} = \frac{V_{C1} - V_{Cd}}{R_d} \quad (25)$$

Now defining states of the converter as follows:

$x_1 = i_{L1}$, $x_2 = i_{L0}$, $x_3 = V_{C1}$, $x_4 = V_{Cd}$, $x_5 = V_{C0}$ and $U = Vin$, $Y = V_0$

Using state space analysis the state space equation for switch ON period (using equation 16 to 20) can be written as

$$\dot{x} = A_1x + B_1U$$

Where $$x = \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \\ x_5 \end{bmatrix} = \begin{bmatrix} i_{L1} \\ i_{Lo} \\ V_{C1} \\ V_{Cd} \\ V_{C0} \end{bmatrix}$$

and $$A_1 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{C_1} & -\frac{1}{R_d} & \frac{1}{R_d} & 0 \\ 0 & 0 & \frac{1}{R_dC_d} & \frac{1}{R_dC_d} & 0 \\ 0 & 0 & 0 & 0 & -\frac{1}{RC_0} \end{bmatrix}, B_1 = \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_0} \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (26)$$

Similarly for switch OFF period (using equation 21 to 25) state space equation can be written as

$$\dot{x} = A_2x + B_2U$$

Where $$A_2 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{L_0} & 0 & 0 \\ 0 & -\frac{1}{C_1} & -\frac{1}{R_dC_d} & \frac{1}{R_dC_d} & 0 \\ 0 & 0 & \frac{1}{R_dC_d} & -\frac{1}{R_dC_d} & 0 \\ 0 & 0 & 0 & 0 & -\frac{1}{RC_0} \end{bmatrix}, B_2 = \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (27)$$

Using the analysis that is described in section IV the control to inductor current transfer functions of the modified converter (with damped network R_d=60Ω, C_d=1μF) can be obtained as equ.28 with power stage parameters given in the section IV.

$$G_{di(damped)}(s) = \frac{283000s^4 + 1.98*10^{10}s^3 + 2.76*10^{14}s^2 + 3.48*10^{18} + 1.4*10^{20}}{s^5 + 52200s^4 + 8.32*10^8s^3 + 2.93*10^{13}s^2 + 9.15*10^{14}s + 1.16*10^{19}} \quad (28)$$

B. Comparison of Frequency Response:

From Fig.6 it can be observed that there is a significant reduction in Q factor at point 2 by using the damping network. The marginal values of the modified converter is founded as: Gain Margin(G.M.)=∞,Phase Margin(P.M.)= 86.5025 with gain crossover frequency (ω_{gc})= ∞ and phase crossover frequency (ω_{pc})= 2.8623*10^5 with four complex poles($p_{1,2}$ at (-0.2233 ±2.4749i)×10^4 and $p_{3,4}$ at (-0.0010 ± 0.0627i)*10^4), a real pole(p_5 at -4.7714×10^4), two complex zeros ($z_{1,2}$ at (0.6680 ± 1.3118i)*10^4) and two real zeros(Z_3 at 0.0040*10^4 and Z_4 at -5.6563*10^4).The marginal value and pole-zero location of the modified converter indicates that the modified system Fig.5 is stable.

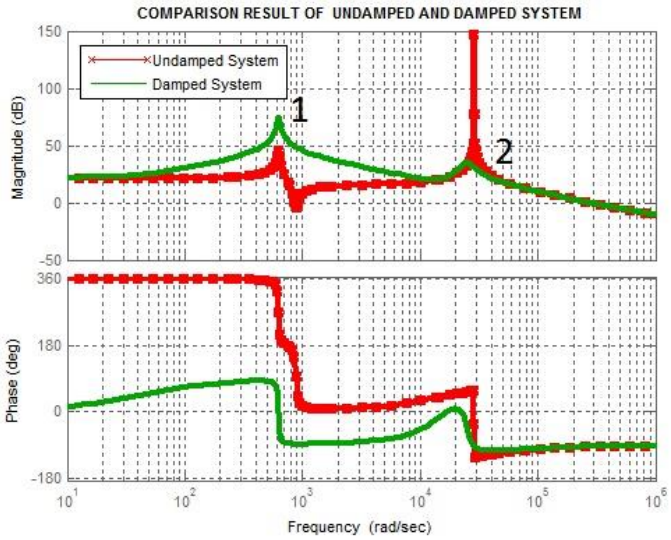

Fig.6 Frequency response comparison of control to inductor model G_{id}(Eq.15 & Equ.28)

7. Simulation Result

To validate the model a comparison is made between the small signal model of the derived (equation-28) and simulated model Fig.5. The result of comparison between the derived and simulated model of control to inductor (G_{id}) in terms of its magnitude response and phase response is shown in Fig. 7(a) and 7(b) which validate the accuracy of the model. For the simulation model the power stage parameters are taken same as that described in section IV.

Figure8 shows the simulated input voltage and current. From the simulated result the power factor is found to be as 0.94 with low THD. Fig.9 shows the switching voltage waveform of S which shows that the switching loss is very Fig.10 shows the simulation result of d.c. output voltage.

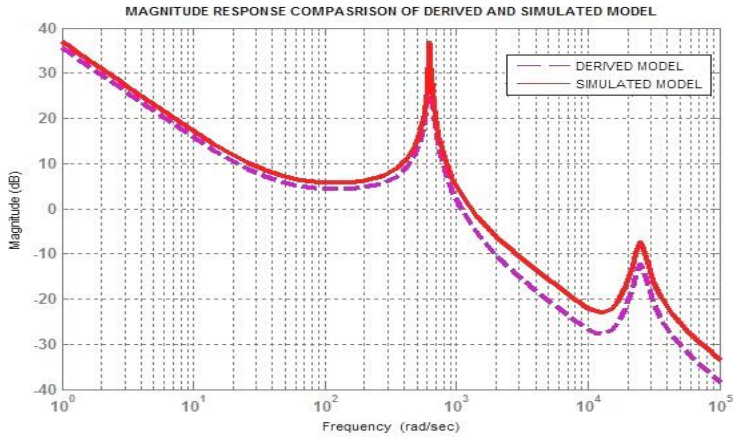

Fig.7a. Frequency response comparison between derived and simulated model of control to inductor model Magnitude response

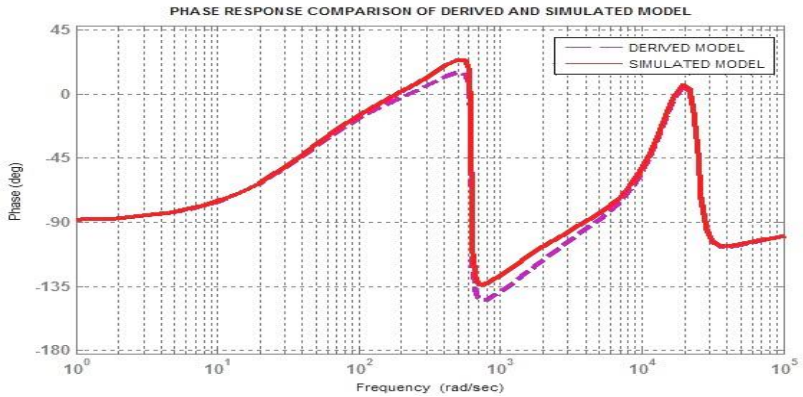

Fig.7.b Frequency response comparison between derived and simulated model of control to inductor model. Phase response

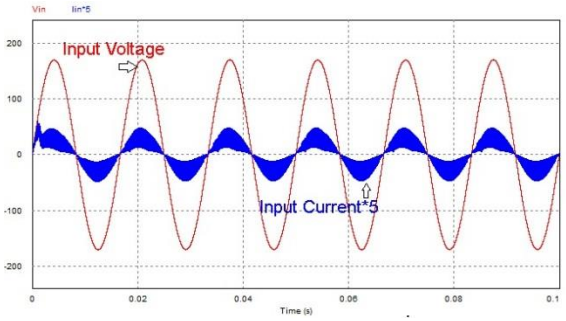

Fig.8 Input voltage and input current simulation result

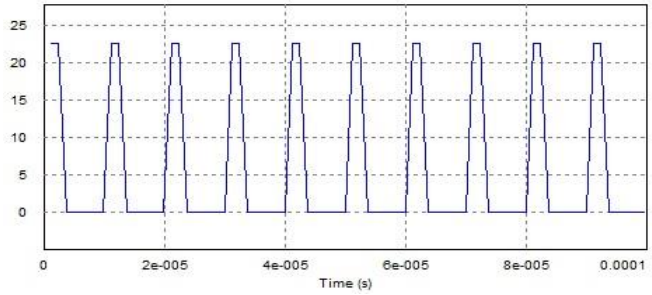

Fig.9 Switching voltage waveform of S

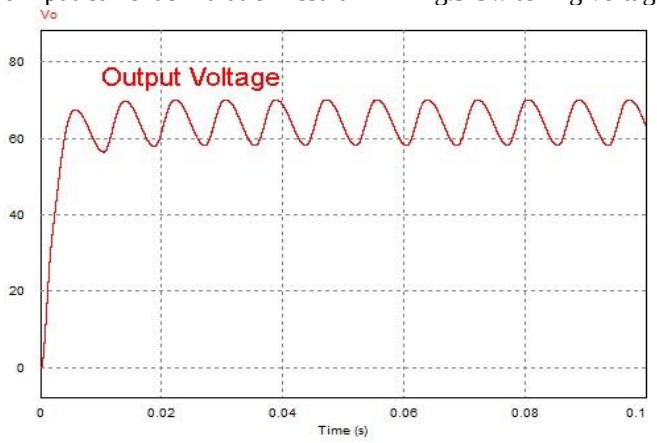

Fig.10 Output voltage simulation result

8. Conclusion

In this paper, modelling and simulation of single switch bridgeless SEPIC PFC converter operating in Continuous conduction mode has been performed using SSA technique. To validate the model the transfer function (e.g. control to inductor current G_{id})is derived for the system with and without damping network and their frequency responses has been obtained. The frequency response of derived model is compared with simulated model (PWM switch model) of G_{id} and has been has been plotted as shown in fig.7.

The result shows that the proposed model is better in stability and accuracy as compared to the original model. Using simulation the waveforms for input voltage and current has been obtained to find the power factor which is 0.94 with low THD and also the dc output voltage waveform is plotted to meet the design of the proposed converter. The efficiency of the converter is found to be 89% at full load condition.

One of the drawbacks of thistopology is the undesired circulating current from the capacitive coupling loop ($C_1$and C_2), shown in Fig. 3 (a) and (b). The circulating current causes power loss but do notsignificantly affects the total efficiency, so, in the proposed work it was not considered. The power factor and efficiency of the proposed converter can be further improved by incorporating the suitable current controllers with the proposed converter.

References

[1] Ahmad J. Sabzali, Esam H. Ismail,Mustafa A. Al-Saffar, and Abbas A. Fardoun, " *New Bridgeless DCM Sepic and Cuk PFC Rectifiers With Low Conduction and Switching Losses*," Industry Applications, *IEEE transcations on*, VOL. 47, NO. 2, MARCH/APRIL 2011*pp. 873-881J.*

[2] Laszlo Huber,YungtaekJang and Milan M. Jovanovic´," *Performance Evaluation of Bridgeless PFC Boost Rectifiers*" Power Electronics,*IEEE transactions on*, VOL. 23, NO. 3, MAY 2008,*pp.1382-1390*

[3] A. J. Sabzali, E. H. Ismail, M. A. Al-Saffar, and A. A. Fardoun, "A *new bridgeless PFC Sepic and Cuk rectifiers with low conduction and switching losses*," in Power Electronics and Drive Systems, 2009. PEDS 2009. *International Conference on*, 2009, *pp. 550-556*.

[4] V. Eng, U. Pinsopon, and C. Bunlaksananusorn, "*Modeling of a SEPIC converter operating in Continuous Conduction Mode*," in Electrical Engineering/Electronics,Computer, Telecommunications and Information Technology, 2009. ECTI-CON 2009.*6th International Conference on, 2009, pp. 136-139*

[5] G. Spiazzi and P. Mattavelli, "*Design criteria for power factor preregulators based on Sepic and Cuk converters in continuous conduction mode*," Industry Applications *Society Annual Meeting, 1994., IEEE Conference*, 1994, vol.2, *pp. 1084-1089*.

[6] A. Hren and P. Slibar, "Full Order Dynamic Model of SEPIC Converter,"*Proc. of the IEEE International Symposium on Industrial Electronics, pp. 553-558, June 2005.*

[7] STMicroelectronics, Application note:TM SEPIC converter in PFC pre-regulator

[8] E. H. Ismail, "*Bridgeless SEPIC Rectifier with Unity Power Factor and Reduced Conduction Losses*," Industrial Electronics, *IEEE Transactions on*, vol. 56, *pp. 1147-1157, 2009.*